What is claimed is:

1. A phase interpolator, to interpolate between a plurality of clock phases, comprising:

   a. a plurality of switching legs coupled to a common output, each including:

      i. a pair of differential switching transistors each having a gate and two additional terminals, one of which is coupled to said common output, the gates coupled to a respective one of said plurality of clock phases and its complement ;

      ii. a tail coupling the other terminal of said switching transistors to ground, said tail made up of a plurality of transistors; and

   b. a load coupling the common output to a voltage.

2. The phase interpolator of claim 1 wherein said plurality of clock phases comprises four phases.

3. The phase interpolator of claim 2 wherein each of said tails comprises four transistors in parallel to make available 16 phases of the reference clock and its complement.

4. The phase interpolator of claim 2 and further including an N bit digital control, where N equals the total number of transistors in said tails, said control having N outputs coupled to respective gates in the transistors in said tails.

5. The phase interpolator of claim 1 wherein said plurality of clock phases include all phases needed for every phase of interpolation.

6. The phase interpolator of claim 4 wherein the size of said tail transistors is chosen such that when a control signal is coupled to turn on said transistor, said transistor operated in a saturated condition without any voltage bias.

7. The phase interpolator of claim 1 wherein said switching transistors are of large enough size to reject some common mode noise due to charge injection at nodes between the tail and switching transistors.

8. The phase interpolator of claim 7 wherein said switching transistors are large enough to load the input clocks such that they have a rise and fall times that are equal to or larger than one quarter of an input clock period.

9. The phase interpolator of claim 1 wherein said load is provided by load transistors and said load transistors and said tail transistors are selected to be of a size to reduce the interpolator output to very small signals.

10. A phase interpolator, to interpolate between four input clock phase signals, said phases including an in-phase signal, a quadrature signal and the complements of said in-phase signal and quadrature signal, comprising:

a. an common output line and a common complemented output line;

b. four switching legs, each including:

i. a pair of differential switching transistors each having a gate, the respective gates coupled respective ones of said plurality of clock phases and their complements, each differential switching transistors coupled to a

respective one of the common output line and the common complemented output line;

ii. a tail coupling the other terminal of said switching transistors to ground, said tail made up of a plurality of transistors; and

c. a load, including at least one transistor, coupling the common output to a voltage.

11. The phase interpolator of claim 10 wherein each of said tails comprises M transistors in parallel to make available N phases of the reference clock and its complement and further including an N bit digital control, where N equals 4 time N, the total number of transistors in said tails, said control having N outputs coupled to respective gates in the transistors in said tails.

12. The phase interpolator of claim 11 wherein said digital control comprises a shift register in which a group of M bits enables M adjacent tail transistors to select one of said phases.

13. The phase interpolator of claim 12 wherein M equals 4.

14. The phase interpolator of claim 10 wherein:

a. the size of said tail transistors is chosen such that when a control signal is coupled to turn on said transistor, said transistor operated in a saturated condition without any voltage bias;

b. the size of said switching transistors is large enough to reject some common mode noise due to charge injection at nodes between the tail and switching transistors and large enough to load the input clocks such that they have a rise and fall times that are equal to or larger than one quarter of an input clock period; and

c. said load transistors and said tail transistors are selected to be of a size to reduce the interpolator output to very small signals.

15. The phase interpolator of claim 14 wherein:

a. the size of said switching transistors is about 30/.32

b. the size of said tail transistors is about 1.3/.32; and

c. the size of said load transistors is about 7/.32.

16. A tracking receiver comprising:

a. a phase and frequency detector having as inputs a remote serial data input and a recovered remote clock output;

b. a local reference clock providing a plurality of clock phases; and

c. a remote clock recovery mechanism comprising:

i. a common output providing said remote recovered clock output;

ii. a plurality of switching legs, each including:

(1) a pair of differential switching transistors each having a gate and two additional terminals, one of which is coupled to said common output, the gates coupled to a respective one of said plurality of clock phases and its complement ;

(2) a tail coupling the other terminal of said switching transistors to ground, said tail made up of a plurality of transistors;

(3) an N bit digital control, where N equals the total number of transistors in said tails, said control receiving a control input from

said phase and frequency having N outputs coupled to respective gates in the transistors in said tails; and

ii. a load coupling the common output to a voltage.

17. The tracking receiver of claim 16 wherein said plurality of clock phases comprises four phases.

18. The tracking receiver of claim 17 wherein each of said tails comprises M transistors in parallel to make available N phases of the reference clock and its complement.

19. The tracking receiver of claim 18 wherein said digital control comprises a shift register in which a group of M bits enables M adjacent tail transistors to select one of said phases.

20. The tracking receiver of claim 19 wherein M equals 4.

21. The tracking receiver of claim 16 wherein:

a. the size of said tail transistors is chosen such that when a control signal is coupled to turn on said transistor, said transistor operated in a saturated condition without any voltage bias;

b. the size of said switching transistors is large enough to reject some common mode noise due to charge injection at nodes between the tail and switching transistors and large enough to load the input clocks such that they have a rise and fall times that are equal to or larger than one quarter of an input clock period; and

c. said load transistors and said tail transistors are selected to be of a size to reduce the interpolator output to very small signals.

22. The tracking receiver of claim 21 wherein:

a. the size of said switching transistors is about 30/.32

b. the size of said tail transistors is about 1.3/.32; and

c. the size of said load transistors is about 7/.32.